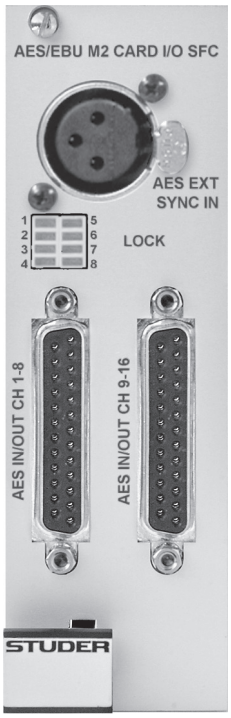
6.3 Digital I/O Cards

6.3.1 AES/EBU M2 Cards (VISTA, OnAir, ROUTE 6000) A949.0454/.0455/.0456



AES/EBU input/output card with 16 Ch I/O, available in 3 different versions:

A949.0454xx without SRCs (Vista only)
A949.0455xx with input SRCs only
A949.0456xx with input and output SRCs (see adjacent picture).

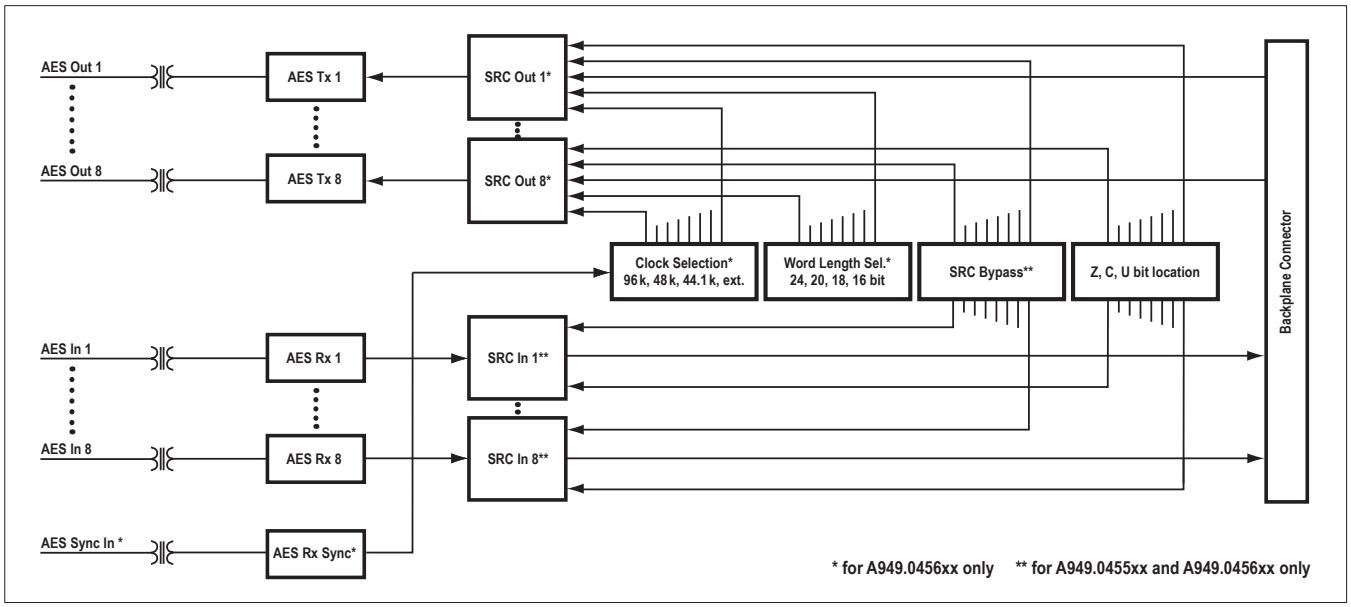
Selectable output sampling rates: 96 kHz, 48 kHz, 44.1 kHz, or external reference (22-108 kHz). Input and output SRCs can individually be bypassed per channel pair. Output dither and word length is selectable for every AES/EBU output to 24, 20, 18 or 16 bit (when the output SRC is enabled). Settings are made with DIP switches. Inputs and outputs are on standard 25-pin D-type connectors (female).

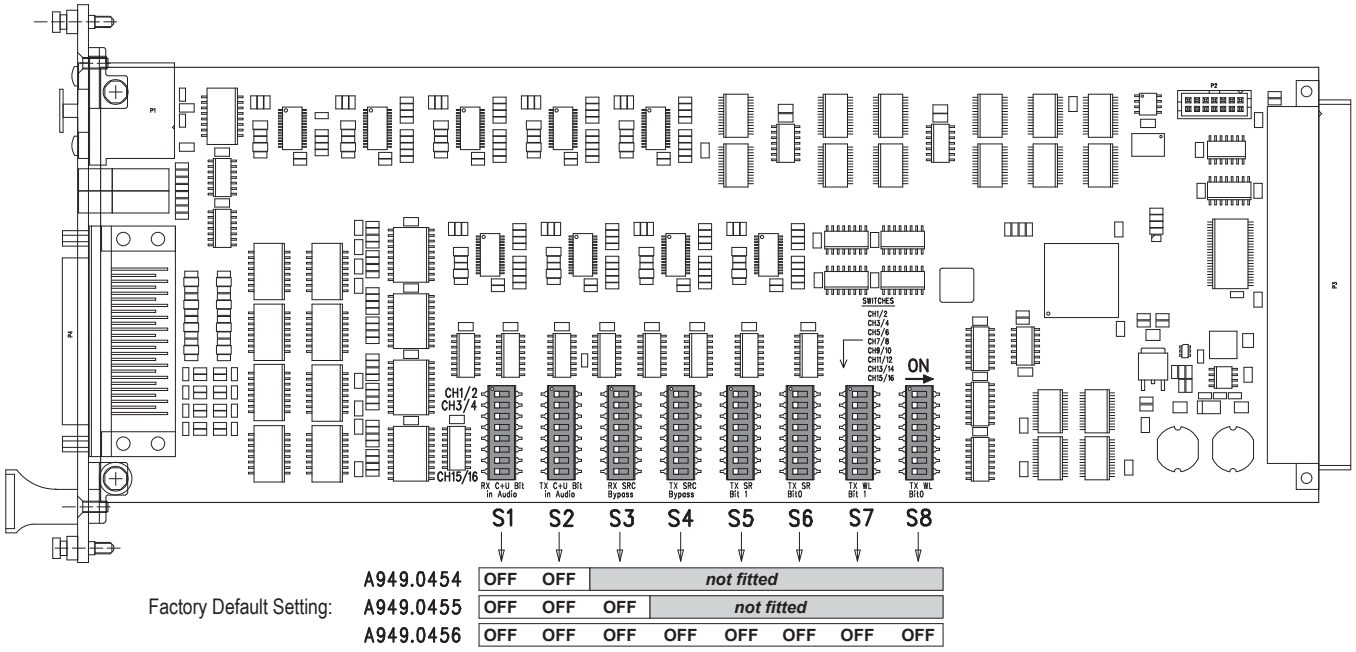
SRC Delay Enabled input and output SRCs each cause a delay (D) that depends on the SRC's input and output sampling rate (f_{S_IN} and f_{S_OUT}). Input and output delays can be calculated using the following formulas.

$$[1]\ f_{S\_IN} > f_{S\_OUT}:\ D = \frac{16}{f_{S\_IN}} + \frac{32}{f_{S\_OUT}}\ [s] \qquad [2]\ f_{S\_OUT} > f_{S\_IN}:\ D = \frac{48}{f_{S\_IN}}\ [s]$$

Examples: *For a 96 kHz input signal and a 48 kHz system clock (i.e., the 'output signal' of the input SRC), input delay is 40 output samples or 0.833 ms (formula [1]). For a 48 kHz system clock (i.e., the 'input signal' of the output SRC) and a 96 kHz output signal, output delay is 96 output samples or 1 ms (formula [2]).*

Input / output impedance		110 Ω
Input sensitivity		min. 0.2 V
Output level (into 110 Ω)		4.0 V
THD + noise		max. –115 dB
SRC range		22-108 kHz
Current consumption	(3.3 V)	A949.0454: 0.43 A/.0455: 0.67 A/.0456: 0.94 A
	(5 V)	0.45 A
Operating temperature		0-40 °C





LEDs **LOCK 1-8** These green LEDs are on if a valid AES/EBU signal is available at the inputs.

DIP Switches

S1 (C+U Bits in Audio) Specifies the usage of the ZCU bits. If OFF, the audio is standard 24 bit PCM; if ON, the LSBs of the audio carry the ZCU bits. This setting both defines at what position the ZCU bits are inserted (receiver) and which bits are used to generate the transmitted ZCU bits (transmitter). Default setting: all OFF.

S2 (C+U Bits Source) If OFF, a static, default ZCU pattern is generated at the transmitter side. If ON, the ZCU bits of the routed source (position depending on setting of S1) are used. Default setting: all OFF.

S3 (Input SRC Bypass) *(A949.0455 and A949.0456 only)* Bypassing (ON) or enabling (OFF) of the SRCs for individual AES/EBU input channels (i.e. audio channel pairs 1+2, 3+4, etc.). Default setting: all OFF.

S4 (Output SRC Bypass) *(A949.0456 only)* Bypassing (ON) or enabling (OFF) of the SRCs for individual AES/EBU output channels (i.e. audio channel pairs 1+2, 3+4, etc.). *For output word length reduction the output SRCs must be enabled. Refer to the paragraph below.* Default setting: all OFF.

S5, S6 (Output Sample Rate) *(A949.0456 only)* Used for setting the sample rate for the AES/EBU output channels (i.e. audio channel pairs 1+2, 3+4, etc.). Corresponding switches on S5 and S6 are used in pairs for each AES/EBU channel, according to the following table and the silkscreen on the PCB. Default setting: All OFF, corresponding to 48 kHz.

S5.x	S6.x	Output Sample Rate
OFF	OFF	48 kHz
OFF	ON	96 kHz
ON	OFF	44.1 kHz
ON	ON	External AES sync

If no valid signal is provided at the **AES EXT SYNC IN** connector but external sync is selected, the output sampling rate will be set to the system clock. Outputs set to 'external' can therefore be used in a very flexible way: Connect

no external sync signal if not necessary, and the output will be clocked with the internal system clock. As soon as an external sync signal is provided to the **AES EXT SYNC IN** connector, the output will automatically be clocked by the extermal sync signal.

S7, S8 (Output Word Length) *(A949.0456 only)* Used for setting the resolution (output word length) for the AES/EBU output channels (i.e. audio channel pairs 1+2, 3+4, etc.). Corresponding switches on S7 and S8 are used in pairs for each AES/EBU channel, according to the following table and the silkscreen on the PCB. Default setting: All OFF, corresponding to 24 bit.

S7.x	S8.x	Output Word Length
OFF	OFF	24 bit
OFF	ON	20 bit
ON	OFF	18 bit
ON	ON	16 bit

Note *For word length reduction the output SRCs must be set to enabled'; if so, the output word length is always 21 bit maximum. Whenever an SRC is enabled, the three least significant bits (LSB) are set to digital zero. This results in the specified dynamic range of 120 dB.*

Special Channel Status and User Bits Data Management

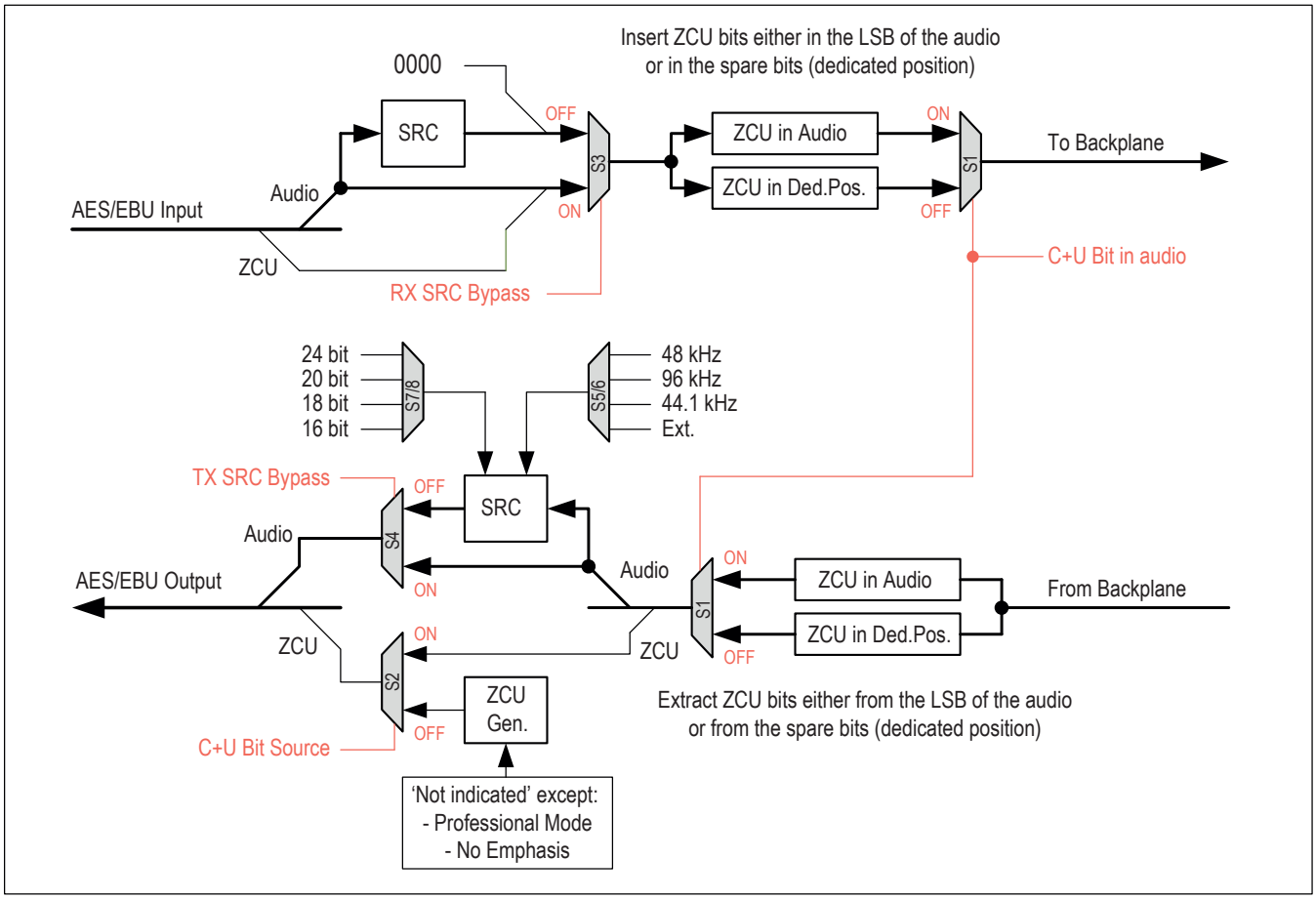
Some intercom systems use a standard AES stream to link control panels to the main base station. In addition to the audio, control data is encoded into the user bits of the AES stream. In order to allow an intercom remote control panel to be transmitted from a Studer stagebox to the base station, a special mode is available on these AES cards.

The channel status and users bits (CU bits) are extracted at the receiver side. Depending on the setting of DIP switch S1, the CU bits are either embedded into the two bottom LSBs of the audio (S1 = ON) or sent to the D21m backplane (S1 = OFF). In addition, the channel status data block start (Z bit) is also embedded into the bottom LSB of the audio to allow recovery of the block start at the destination AES transmitter. If the ZCU bits are embedded into the audio, the audio word length is reduced to 20 bits.

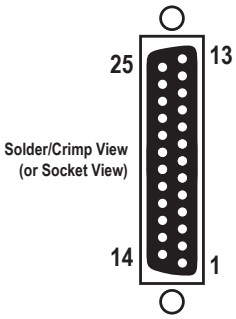
Note *The resulting audio data contains non-audio information in the four bottom bits of the 24 bit audio word and thus is no longer fully PCM. This non-PCM signal may be routed through Studer routers and the routing part of all Studer audio mixing systems, but will not pass through any active processing such as a channel path or sample rate converter.*

At the output side, an additional DIP switch (S2) allows the selection of the source of the transmitted ZCU bits. Either a default, static pattern (S2 = OFF) or the ZCU bits available from the backplane are encoded (S2 = ON). If S2 is ON then the bits from the position specified with S1 are encoded.

The following diagram illustrates the various DIP switches and their effect upon the data path.



Connector Pin Assignment



AES IN/OUT (2 × 25pin D-type, female, UNC 4-40 thread)

Pin	Signal 'CH 1-8'	Signal 'CH 9-16'	Pin	Signal 'CH 1-8'	Signal 'CH 9-16'
1	CH 7/8 out +	CH 15/16 out +	14	CH 7/8 out –	CH 15/16 out –
2	CH 7/8 out screen	CH 15/16 out screen	15	CH 5/6 out +	CH 13/14 out +
3	CH 5/6 out –	CH 13/14 out –	16	CH 5/6 out screen	CH 13/14 out screen
4	CH 3/4 out +	CH 11/12 out +	17	CH 3/4 out –	CH 11/12 out –
5	CH 3/4 out screen	CH 11/12 out screen	18	CH 1/2 out +	CH 9/10 out +
6	CH 1/2 out –	CH 9/10 out –	19	CH 1/2 out screen	CH 9/10 out screen
7	CH 7/8 in +	CH 15/16 in +	20	CH 7/8 in –	CH 15/16 in –
8	CH 7/8 in screen	CH 15/16 in screen	21	CH 5/6 in +	CH 13/14 in +
9	CH 5/6 in –	CH 13/14 in –	22	CH 5/6 in screen	CH 13/14 in screen
10	CH 3/4 in +	CH 11/12 in +	23	CH 3/4 in –	CH 11/12 in –
11	CH 3/4 in screen	CH 11/12 in screen	24	CH 1/2 in +	CH 9/10 in +
12	CH 1/2 in –	CH 9/10 in –	25	CH 1/2 in screen	CH 9/10 in screen
13	n.c.	n.c.			